IN THE SPECIFICATION

Amend paragraphs 3, 7, 8, 41, 55, 58, 59, 61, 72, 74, 77, 79 - 81, 83, 87, 88, 92, 94 - 97, 100, 101, 105, 113, 120, 126, 132, 134, and 137 as follows:

[0003] A floating-gate FET has a threshold voltage, referred to here as the programmable threshold voltage, which can be adjusted subsequent to FET manufacture for controlling the FET's operational characteristics. During FET operation, one of the source/drain regions ~~region~~ functions as the source while the other functions as the drain. A control voltage is applied between the control gate and the source. With suitable potentials applied to other parts of the FET, the programmable threshold voltage is the value of the control voltage at which the FET switches between on and off conditions.

[0007] The floating-gate FET is in a first condition, e.g., an erased condition, when its programmable threshold voltage is (a) less than a first transition value V_{T1} if the FET is of n-channel type and (b) greater than $-V_{T1}$ if the FET is of p-channel type. The FET is in a second condition, e.g., a programmed condition, when its programmable threshold voltage is ~~greater~~ (a) greater than a second transition value V_{T2} if the FET is of n-channel type and (b) less than $-V_{T2}$ if the FET is of p-channel type where V_{T2} exceeds or equals V_{T1}. A first body voltage at a body node is converted into a second body voltage applied to the body region. A first control voltage at a control node is converted into a second control voltage applied to the control gate.

[0008] The control technique of the invention entails initially placing the first body and first control voltages at respective body and control conditioning values different from each other such that the second body and second control voltages cause the floating-gate FET to be in the first condition with its programmable threshold voltage (a) less than V_{T1} if the FET is of n-channel type or (b) greater than $-V_{T1}$ if the FET is of p-channel type regardless of the immediately previous condition of the FET, i.e., regardless of whether the FET was in the first or second condition immediately previous to the voltage-placing operation. Suitable conditioning circuitry is utilized to perform the voltage-placing operation.

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[0041] After erasure is completed, information can be written into the EPROM sector of Fig. 1. Writing is accomplished by performing a programming operation on certain selected ones of floating-gate FETs 20 to place those selected FETs 20 in the ~~their~~ second, or programmed, condition at logic "0" with their programmable threshold voltages (a) greater

than V_{T2} if FETs 20 are of n-channel type or (b) less than $-V_{T2}$ if FETs 20 are of p-channel type. At the end of a typical programming/write (or simply "programming") operation, some of FETs 20 are typically in the programmed condition at logic "0" while others remain in the erased condition at logic "1". A read operation can now be performed to determine the information stored in various ones of FETs 20.

[0055] An erasure operation consists of a main erasure portion and an erasure voltage discharge portion. Control-line discharge circuitry 36 is provided with four signals that variously control the timing of the main erasure and discharge portions of an erasure operation: an erasure/discharge voltage signal V_{ED}, an erasure-only voltage signal V_{EO}, an erasure-voltage-detection voltage signal V_{IM}, and a longer-duration erasure-voltage-detection voltage signal V_{IT}. Erasure/discharge voltage V_{ED} establishes the full length, including the discharge portion, of an erasure interval. Erasure-only voltage V_{EO} establishes the length of the main erasure portion of an erasure interval. Erasure-only voltage V_{EO} is <u>also</u> provided to common discharge circuitry 46. Low-voltage generator 34 and discharge circuitries 36 and 46 cooperate as described below to produce erasure control voltage V_{CE}. Erasure-voltage-detection voltages V_{IM} and V_{IT} are, as discussed further below, both generated from an additional erasure-voltage-detection voltage signal.

[0058] Each control-line voltage V_{CL} is provided from control-line decoder 32 so as to settle at one of the following four values (running from highest to lowest) during EPROM operation: V_{CPH}, V_{DD}, V_{SS}, and V_{CEL}, <u>e.g., typically respectively 10, 3, 0, and -10 V</u>. When control-line selection signals V_{CLS} are set at values that select the EPROM sector of Fig. 1, further setting signals V_{CLS} at values that select erasure cause control-line signals V_{CL} to go from V_{SS} downward to low erasure control conditioning value V_{CEL} on all control lines 62 for the illustrated EPROM sector during the main portion of the erasure operation. Control-line voltages V_{CL} on control lines 62 in the illustrated EPROM sector are subsequently returned to V_{SS} during the discharge portion of the erasure operation in the inventive manner described below.

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[0059] Setting control-line selection signals V_{CLS} at values that select programming causes control-line voltage V_{CL} to be provided at high programming voltage V_{CPH} on control line 62 connected to FETs 20 in the selected cell row and typically in three other cell rows. Control-line voltages V_{CL} are at V_{SS} on all other control lines <u>62</u> ~~52~~ for the illustrated EPROM sector. With select-line selection signals V_{SLS} to select/source decoder 30 being

simultaneously set at values that select programming for the sector of Fig. 1, source-line voltage V_{SL} is provided at high programming value V_{SPH} on source line 52 connected to FETs 20 in the selected cell row and typically to three other cell rows that differ from the additional three cell rows that receive high control-line programming voltage V_{CPH} at the same time as the selected cell row. As determined by bit-line voltages V_D on bit lines 26, certain of FETs 20 in the selected row undergo programming to logic "0". No FET 20 in any of the other rows undergoes programming to logic "0" because none of them receives both of high programming voltages V_{SPH} and V_{CPH} at the same time as the selected row.

[0061] Body-line decoder 40 receives an erasure body voltage signal V_{BE} on a line 64 connected to high-voltage generator 42 normally implemented with a charge pump. High-voltage generator 42 adjusts erasure body voltage V_{BE} in response to generator control signal V_{BHC}. Body-line discharge circuitry 44 is connected by way of a line 68 ~~66~~ to a body node N_B on line 64. Common discharge circuitry 46 is similarly connected through a line 66 to body node N_B. Analogous to what was said above about lines 56 and 58 relative to control node N_C, lines 66 and 68 are actually typically connected to line 64 at two different places and therefore at two different nodes on line 64 but, because these two nodes on line 64 are substantially equivalent electrically, they are treated here as body node N_B at which voltage V_{BE} is present. As discussed below, voltage V_{BE} varies from an erasure body discharge value, typically V_{DD}, to a high erasure conditioning body value V_{BEH} considerably greater than V_{DD}. Erasure body conditioning value V_{BEH} is typically 5 V above V_{DD} and thus typically 8 V above V_{SS}.

[0072] The low V_{EO} and high V_{IM} values at time t_0 cause body-line discharge circuitry 44 to electrically connect line 66 to the V_{DD} supply. Due to the low ~~high~~ V_{EO} value, the voltage on line 68 is not significantly affected by common discharge circuitry 46 at time t_0. Generator control signal V_{BHC} is initially at a value that causes high-voltage generator 42 to be turned off. At time t_0, generator 42 therefore does not significantly affect the voltage on line 64. Consequently, body node N_B at the intersection of lines 64, 66, and 68 is effectively electrically disconnected from common discharge circuitry 46 and high-voltage generator 42 at time t_0.

[0074] The ~~combination of the high V_{EI} value at time t_0 and the~~ V_{BLS} selection-signal values that result in the selection of the illustrated EPROM sector at time t_0 cause ~~causes~~ body line 70 for the selected sector to be electrically disconnected from the V_{SS} supply by the

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hard electrical path through body-line decoder 40. However, line 70 for the selected sector remains electrically connected to the V_{SS} supply by way of the soft electrical path through decoder 40. Hence, body-line voltage V_{BL} on line 70 for the illustrated sector equals V_{SS} at time t_0. Line 70 for the illustrated sector is also electrically disconnected from line 64 ~~68~~ at time t_0 so that decoder 40 does not affect erasure body voltage V_{BE} at body node N_B. Since node N_B is initially electrically connected through line 66 and body-line discharge circuitry 44 to the V_{DD} supply, voltage V_{BE} equals V_{DD}, the preferred erasure body conditioning value, at time t_0.

[0077] Prior to selecting the illustrated EPROM sector for erasure, control lines 62 for the selected sector are typically connected to the V_{SS} supply by an electrical path through control-line decoder 32. At time t_0, the combination of the low V_{IM} value, the high V_{IT} value, and the V_{CLS} selection-signal values that lead to the selection of the illustrated EPROM sector (a) causes ~~cause~~ this electrical path to be broken so that control lines 62 for the illustrated sector are no longer electrically connected through decoder 32 to the V_{SS} supply and (b) simultaneously causes ~~cause~~ decoder 32 to electrically connect line 54 to control lines 62 for the illustrated sector. Since erasure control voltage V_{CE} is present at control node N_C on line 54 and since node N_C is initially connected through line 56 and control-line discharge circuitry 36 to the V_{SS} supply, erasure control voltage V_{CE} and control-line voltages V_{CL} for the illustrated sector all equal V_{SS}, the preferred erasure control discharge value, at time t_0.

[0079] The low V_{EI} value at time t_1 (a) causes body line 70 for the illustrated EPROM sector to be fully electrically disconnected from the V_{SS} supply through body-line decoder 40, i.e., line ~~lines~~ 70 for the selected sector now becomes ~~become~~ electrically disconnected from the V_{SS} supply via the soft electrical path through decoder 40, and (b) simultaneously causes ~~cause~~ decoder 40 to electrically connect line 64 to body line ~~lines~~ 70 for the illustrated sector. Erasure body voltage V_{BE} then pulls body-line voltage V_{BL} for the selected sector upward from V_{SS} to V_{BEH}. Erasure body voltage V_{BE} is thereby converted into body-line voltage V_{BL} for the selected sector during erasure.

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[0080] The high V_{ED} and V_{EO} values at time t_1 cause line 56 to be electrically disconnected from the V_{SS} supply through control-line discharge circuitry 36. This applies to both the strong-ground and weak-ground circuitries in control-line discharge circuitry ~~decoder~~ 36 when it so implemented. With control node N_C substantially electrically isolated from control-line discharge circuitry 36 and common discharge circuitry 46, generator

control signal V_{CLC} changes to a value that causes low-voltage generator 34 to turn on. This enables generator 34 to pump erasure control voltage V_{CE} downward from control discharge value V_{SS} to low control conditioning value V_{CEL}. Line 54 remains electrically connected through control-line decoder 32 to control lines 62 ~~line 64~~ for the selected EPROM sector. Erasure control voltage V_{CE} then pulls control-line voltages V_{CL} for the selected sector downward from V_{SS} to V_{CEL}. In this way, erasure control voltage V_{CE} is converted into control-line voltages V_{CL} for the selected sector during erasure.

[0081] Erasure control voltage V_{CE} is detected by suitable voltage-detection circuitry (not shown) which produces the above-mentioned additional erasure-voltage-detection voltage (not shown in Fig. 4) ~~2)~~ and causes the additional detection voltage to make transitions when voltage V_{CE} passes (upward and downward) through a specified detected value V_{CEX} between V_{SS} and low value V_{CEL}. Detected value V_{CEX} is typically 5 V below V_{SS}.

[0083] Erasure control voltage V_{CE} and control-line voltages V_{CL} for the illustrated EPROM sector reach low control conditioning value V_{CEL} approximately simultaneously at a time subsequent to time t_3. Erasure body voltage V_{BE} and body-line voltage V_{BL} for the selected sector reach high body conditioning value V_{BEH} approximately simultaneously at a time subsequent to time t_1. With all of bit-line voltages V_D and source-line voltages V_{SL} for the illustrated EPROM sector still floating and with all of select-line voltages V_{SG} for the illustrated sector still at V_{ITM}, the combination of the high V_{BEH} value of body-line voltage V_{BL} for the illustrated sector and the low V_{CEL} ~~V_{CE}~~ value of control-line voltages V_{CL} for the illustrated sector causes all of floating-gate memory FETs 20 to be erased simultaneously to logic "1".

[0087] The erasure body discharge value is greater than or equal to the erasure control discharge value. Preferably, the body discharge value is somewhat greater than the control discharge value. In a preferred implementation, the body discharge value is high supply value V_{DD} as indicated above while the control discharge value is low supply value V_{SS} as likewise indicated above. Supply values V_{DD} and V_{SS} are respectively used as the body and control discharge values in the material below. The body discharge value exceeds the control discharge value by the supply-voltage range V_{DD} - V_{SS}, typically 3 V.

[0088] Line 64 continues to be electrically connected to body line 70 for the illustrated EPROM sector. Accordingly, erasure body voltage V_{BE} starts to pull body-line voltage V_{BL}

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~~V_{BE}~~ for the illustrated sector downward. Line 54 likewise continues to be electrically connected to control lines ~~line~~ 62 for the illustrated sector. Erasure control voltage V_{CE} thereby starts pulling control-line voltages V_{CL} for the illustrated sector upward to control discharge value V_{SS}.

[0092] The voltage-generation circuitry which generates detection voltages V_{IM} and V_{IT} delays detection voltage V_{IT} by a selected further time delay, typically 100 ns, from detection voltage V_{IM} so that detection voltage V_{IT} transitions high at time t_6 slightly later than time t_5 while erasure control voltage V_{CE} continues ~~continue~~ moving upward to control discharge value V_{SS}. The high V_{IT} value prepares control-line discharge circuitry 36 for the subsequent high-to-low transition in erasure/discharge voltage V_{ED} but does not affect erasure body voltage V_{BE}. The V_{IM} transition at time t_5 and the V_{IT} transition at time t_6 prepare control-line decoder 32 for the completion of erasure but do not affect the electrical connection of line 54 to control lines 62 for the illustrated EPROM sector.

[0094] The erasure operation specifically, the discharge portion, ends when erasure/discharge voltage V_{ED} transitions low at time t_7. When control-line discharge circuitry 36 contains strong-ground and weak-ground circuitries, the low V_{ED} value causes line 56 to be electrically connected to the V_{SS} supply through the strong-ground circuitry. Inasmuch as the resistor(s) in the current path from line 56 through the weak-ground circuitry to the V_{SS} supply could cause erasure control ~~body~~ voltage V_{CE} ~~V_{BE}~~ to vary somewhat from V_{SS}, the strong-ground circuitry holds voltage V_{CE} ~~V_{BE}~~ close to V_{SS}.

[0095] Body-line selection signals V_{BLS} and control-line selection signals V_{CLS} subsequently return to values that deselect the illustrated EPROM sector. The combination of the then-existing high V_{EI} value and the V_{BLS} values that deselect the illustrated sector causes body line 70 for the illustrated sector to be electrically connected to the V_{SS} supply by way of the hard electrical path through body-line decoder 40. This enables body-line voltage V_{BL} on line 70 for the illustrated sector to be held close to V_{SS}. At the same time, the then-existing low V_{IM} and high V_{IT} values in combination with the V_{CLS} values that deselect the illustrated sector (a) cause control-line decoder 32 to electrically disconnect line 54 from control lines 62 for the illustrated sector and (b) simultaneously cause control lines ~~line~~ 62 for the illustrated sector to be electrically connected to the V_{SS} supply by way of the above-mentioned electrical path through decoder 32. As a result, decoders 40 and 32 are returned to the conditions that they were in prior to selection of the illustrated sector.

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[0096] The (rising/falling) directions in which voltages V_{ED}, V_{EO}, V_{EI}, V_{IM}, and V_{IT} variously make transitions at times ~~time~~ t_0 - t_7 are exemplary. Each of voltages V_{ED}, V_{EO}, V_{EI}, V_{IM}, and V_{IT} could be replaced with a voltage signal having transitions in the opposite directions to those ~~direction to that~~ described above and depicted in Fig. 4 by appropriately adding one or more inverters to, or removing one or more inverters from, the output circuitry that provides each of these voltage signals or the input circuitry that receives each of these signals.

[0097] Fig. 5 presents voltage timing curves that facilitate an understanding of the benefits of the EPROM circuitry of Fig. 1. Fig. 5 specifically illustrates how erasure body voltage V_{BE} and erasure control voltage V_{CE} could vary during erasure if common discharge circuitry 46 were absent and if the discharge of voltages V_{BE} and V_{CE} respectively to V_{DD} and V_{SS} during the discharge portion of erasure were respectively controlled by body-line and control-line discharge circuitries similar to discharge circuitries 44 and 36 but modified to separately start discharging generally at time t_4 rather than providing discharge assistance, as in the invention, starting ~~by starting discharging~~ at time t_5 after common discharge circuitry 46 has initiated the simultaneous discharge of voltages V_{BE} and V_{CE} at time t_4.

[0100] The middle two curves in Fig. 5 illustrate how the V_{BE} ~~VBE~~ and V_{CE} ~~VCE~~ curves would generally appear during erasure if erasure body voltage V_{BE} ~~VBE~~ started to discharge first. Erasure control voltage V_{CE} ~~VCE~~ might then initially move in the wrong direction as indicated at area 80. If erasure control voltage V_{CE} ~~VCE~~ started to discharge first as represented by the bottom two curves in Fig. 5, erasure body voltage V_{BE} ~~VBE~~ might initially move in the wrong direction as indicated at area 82. The initial wrong direction movement of voltage V_{CE} ~~VCE~~ (if voltage V_{BE} ~~VBE~~ starts to discharge first) or voltage V_{BE} ~~VBE~~ (if voltage V_{CE} ~~VCE~~ starts to discharge first) ~~discharge) first~~ could damage the EPROM or impair its operation. The EPROM circuitry of Fig. 1 avoids this wrong-direction discharge problem by utilizing common discharge circuitry 46 to force voltages V_{BE} ~~VBE~~ and V_{CE} ~~VCE~~ to start discharging simultaneously in their respective proper directions.

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[0101] The present invention is not limited to memory cells implemented with split-gate floating-gate FETs ~~FETs, e.g., split-gate devices~~ having both control gates CG and select gates SG. For instance, the invention encompasses memory cells implemented with split-gate floating-gate FETs having control gates CG but not select gates SG. Figs. 6a and 7a depict one such split-gate FET in which floating gate FG overlies part of the channel

portion and extends partially over source S while control gate CG overlies floating gate FG, extends ~~partially~~ over the remainder of the channel portion, and extends partially over drain D. As with split-gate FET 20 having select gate SG, inversion layer IV below floating gate FG forms along only part of the upper surface of the channel portion in the memory cell of Figs. 6a and 7a.

[0105] The high V_{EO} value resulting from the low-to-high transition in erasure-only voltage V_{EO} at time t_1 at the beginning of the main portion of the erasure operation causes FETs N1, N3, N5, and P2 to turn off. FETs N2, N4, N6, and P1 turn on. FET P3 remains on. ~~FET N5 temporarily turns off.~~ The off condition of FET N5 further breaks the electrical path through elements N5, P3, R1, and N7 for electrically connecting nodes N_B and N_C to each other.

[0113] The low-to-high transition in detection voltage V_{IM} at time t_3 during the main portion of the erasure operation does not affect the condition of any of FETs N11, N12, P11, P12, and P13. Because voltage V_{IM} went high at time t_3, the high-to-low transition of erasure-only voltage V_{EO} at time t_4 likewise does not affect the on/off condition of any of FETs N11, N12, P11, P12, and P13. That is, FETs N12, P11, and P13 are still off to effectively electrically disconnect body-line <u>discharge</u> circuitry 44 from body node N_B.

[0120] During the discharge portion of the erasure operation, the high-to-low transition in detection voltage V_{IM} at time t_5 causes FETs P21 and N22 to turn on. FETs N21, N23, N24, and P22 remain off. The on condition of FET N22 enables soft-ground circuitry 110 to electrically connect control node N_C to the V_{SS} supply by way of a soft electrical path through line 56, <u>FET N22,</u> ~~FET 22,~~ and resistor R12. Circuitry 110 thereby assists common discharge circuitry 46 in pulling erasure control voltage V_{CE} to control discharge value V_{SS}. FET N22 functions as a switch for enabling circuitry 110 to make/break the soft electrical path through elements N22 and R12 for connecting node N_C to the V_{SS} supply. Resistor R12 limits the current along this path to prevent damage to the EPROM.

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[0126] Fig. 13 presents internal details for an embodiment of a control-line sector decoder 150 utilized in control-line decoder 32 for the EPROM sector illustrated in Fig. 1. Control-line sector decoder 150 consists of n-channel FETs N31, N32, N33, N34, and N35, p-channel FETs P31, P32, P33, P34, P35, and P36, an AND gate 152, <u>and NOR gates 154 and</u> ~~a NAND gate 154, and a NOR gate~~ 156 connected as shown. FETs N31, N32, P32, and

P33 form a latch 158 that provides a latch voltage signal V_{LS} on a line 160 connected to the gate electrodes of FETs N33, P35, and N35. The state of latch 158 is controlled through FETs P31 and P34. Intermediate control-line voltage V_{CI} is provided on a line 162.

[0132] FET N33 also turns off. FETs P35 and N34 ~~N344~~ turn on. FET P36, which had been turned on when erasure control voltage V_{CE} was below V_{SS} while the EPROM sector illustrated in Fig. 1 was unselected but which turned off when voltage V_{CE} returned to V_{SS}, is now turned off and likewise ceases to electrically connect line 162 to the V_{SS} supply. Instead, line 162 ~~line 62~~ is electrically connected through FET N34 to control node N_C on line 54. At time t_0, intermediate control-line voltage V_{CI} equals voltage V_{CE} which is then at V_{SS}.

[0134] As erasure control voltage V_{CE} at control node N_C moves downward toward control conditioning value V_{CEL} starting at time t_1 at the beginning of the main portion of the erasure operation, latch voltage V_{LS} also moves downward toward V_{CEL}. This occurs because FET N32 is turned on and electrically connects line 160 that carries voltage V_{LS} to line 54 that carries voltage V_{CE} while FETs N35 and P36 are turned off to isolate line 160 from the V_{SS} supply. FET N33 ~~FET N35~~ remains off. Even though detection voltage V_{IT} transitions low at time t_2 during the main erasure portion, latch voltage V_{LS} falls sufficiently from time t_1 to time t_2 that FETs P35 and N34 remain on while FETs N33, N35, and P36 remain off.

[0137] Body-line decoder 40 contains LMN body-line sector decoders, one for each sector 140_{jk} of each mat 130_i. The internal details of an embodiment of one such body-line sector decoder 170 are presented in Fig. 14. Body-line sector decoder 170 consists of n-channel FETs N41, N42, N43, and N44, p-channel FETs P41, P42, and P43, a NAND ~~NOR~~ gate 172, and a NOR ~~NAND~~ gate 174 connected as shown.

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